



GENERAL DESCRIPTION



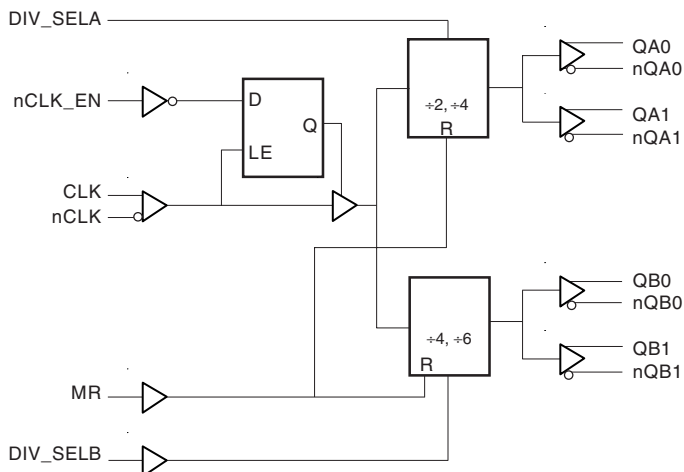
The ICS87339-01 is a low skew, high performance Differential-to-3.3V LVPECL / ECL Clock Generator/Divider and a member of the HiPerClockSTM family of High Performance Clock Solutions from ICS. The ICS87339-01 has one differential clock input pair. The CLK, nCLK pair can accept most standard differential input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS87339-01 ideal for clock distribution applications demanding well defined performance and repeatability.

FEATURES

- Two divide by 2/4 differential 3.3V LVPECL outputs; two divide by 4/6 differential 3.3V LVPECL outputs
- One differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum input frequency: 1GHz
- Translates any single ended input signal (LVCMOS, LVTTTL, GTL) to LVPECL levels with resistor bias on nCLK input
- Output skew: 35ps (maximum)
- Part-to-part skew: 385ps (maximum)
- Bank skew: Bank A - 30ps (maximum)
Bank B - 25ps (maximum)
- Propagation delay: 2.1ns (maximum)
- LVPECL mode operating voltage supply range: $V_{CC} = 3V$ to $3.6V$, $V_{EE} = 0V$
- ECL mode operating voltage supply range: $V_{CC} = 0V$, $V_{EE} = -3.6V$ to $-3V$
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free RoHS compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT

Vcc	1	20	Vcc
nCLK_EN	2	19	QA0
DIV_SELB	3	18	nQA0
CLK	4	17	QA1
nCLK	5	16	nQA1
RESERVED	6	15	QB0
MR	7	14	nQB0
Vcc	8	13	QB1
nc	9	12	nQB1
DIV_SELA	10	11	VEE

ICS87339-01
20-Lead SOIC, M Package
7.5mm x 12.8mm x 2.25
package body
Top View



TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 8, 20	V _{CC}	Power		Positive supply pins.
2	nCLK_EN	Input	Pulldown	Clock enable.
3	DIV_SELB	Input	Pulldown	Selects divide value for Bank B outputs as described in Table 3. LVCMOS / LVTTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup	Inverting differential clock input.
6	RESERVED	Reserve		Reserve pin.
7	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low, and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
9	nc	Unused		No connect.
10	DIV_SELA	Input	Pulldown	Selects divide value for Bank A outputs as described in Table 3. LVCMOS / LVTTTL interface levels.
11	V _{EE}	Power		Negative supply pin.
12, 13	nQB1, QB1	Output		Differential output pair. LVPECL interface levels.
14, 15	nQB0, QB0	Output		Differential output pair. LVPECL interface levels.
16, 17	nQA1, QA1	Output		Differential output pair. LVPECL interface levels.
18, 19	nQA0, QA0	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ

TABLE 3. CONTROL INPUT FUNCTION TABLE

Inputs				Outputs			
MR	nCLK_EN	DIV_SELA	DIV_SELB	QA0, QA1	nQA0, nQA1	QB0, QB1	nQB0, nQB1
1	X	X	X	LOW	HIGH	LOW	HIGH
0	1	X	X	Not Switching	Not Switching	Not Switching	Not Switching
0	0	0	0	÷2	÷2	÷4	÷4
0	0	0	1	÷2	÷2	÷6	÷6
0	0	1	0	÷4	÷4	÷4	÷4
0	0	1	1	÷4	÷4	÷6	÷6

NOTE: After nCLK_EN switches, the clock outputs stop switching following a rising and falling input clock edge.

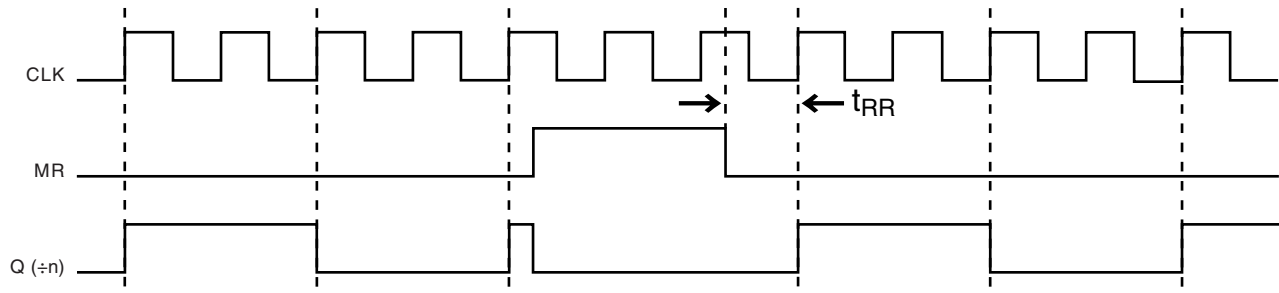


FIGURE 1A. MR TIMING DIAGRAM

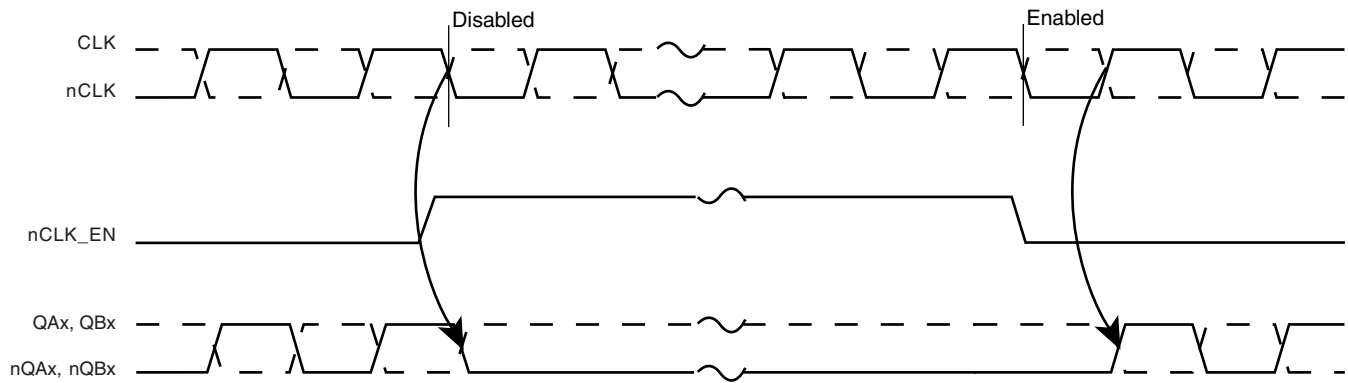


FIGURE 1B. nCLK_EN TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, $V_{EE} = 0$)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, $V_{CC} = 0$)
Inputs, V_I (LVPECL mode)	-0.5V to $V_{CC} + 0.5V$
Inputs, V_I (ECL mode)	0.5V to $V_{EE} - 0.5V$
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sink/Source, I_{BB}	$\pm 0.5mA$
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	46.2°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.0	3.3	3.6	V
I_{EE}	Power Supply Current				105	mA

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	nCLK_EN, MR, DIV_SELA, DIV_SELB $V_{IN} = V_{CC} = 3.6V$			150	μA
I_{IL}	Input Low Current	nCLK_EN, MR, DIV_SELA, DIV_SELB $V_{IN} = 0V, V_{CC} = 3.6V$	-5			μA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	$V_{IN} = V_{CC} = 3.6V$		5	μA
		CLK	$V_{IN} = V_{CC} = 3.6V$		150	μA
I_{IL}	Input Low Current	nCLK	$V_{IN} = 0V, V_{CC} = 3.6V$	-150		μA
		CLK	$V_{IN} = 0V, V_{CC} = 3.6V$	-5		μA
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: For single ended applications, the maximum input voltage for CLK, nCLK is $V_{CC} + 0.3V$.

NOTE 2: Common mode voltage is defined as V_{IH} .



TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = 3.3V \pm 0.3V$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				1	GHz
t_{PD}	Propagation Delay to Output; NOTE 1	CLK to Q (Diff)	1.6		2.1	ns
$t_{sk(o)}$	Output Skew; NOTE 2, 5			20	35	ps
$t_{sk(b)}$	Bank Skew; NOTE 3, 5	Bank A		20	30	ps
		Bank B		12	25	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 4, 5				385	ps
t_S	Setup Time	nCLK_EN to CLK	350			ps
t_H	Hold Time	CLK to nCLK_EN	100			ps
t_{RR}	Reset Recovery Time				400	ps
t_{PW}	Minimum Pulse Width	CLK	550			ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		600	ps
odc	Output Duty Cycle		48		52	%

All data taken with outputs ÷4.

All parameters measured up to 1GHz unless noted otherwise.

This device does not add measureable jitter.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

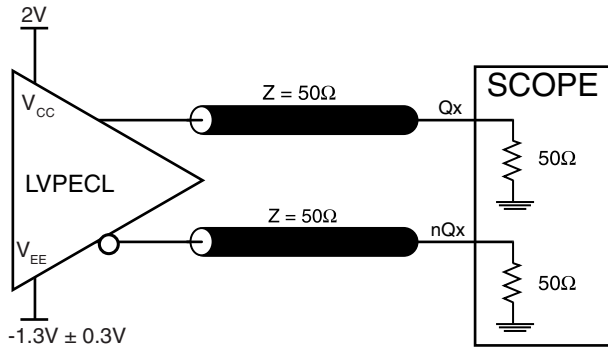
NOTE 3: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

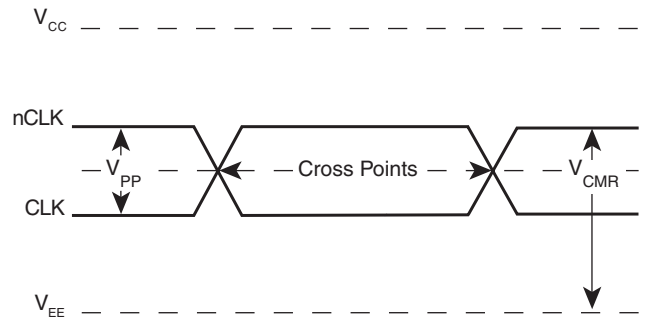
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.



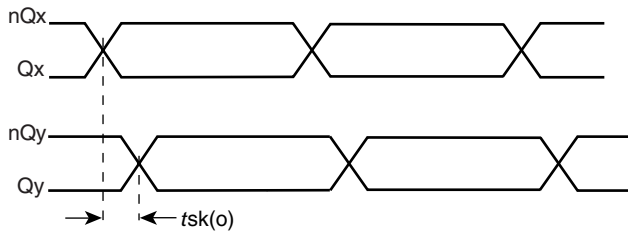
PARAMETER MEASUREMENT INFORMATION



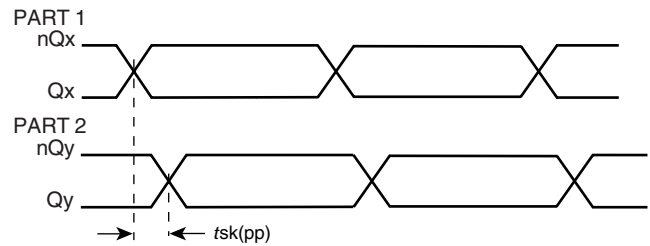
3.3V OUTPUT LOAD AC TEST CIRCUIT



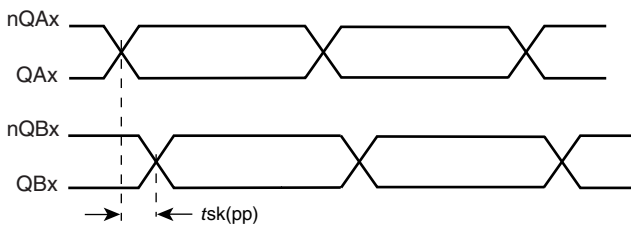
DIFFERENTIAL INPUT LEVEL



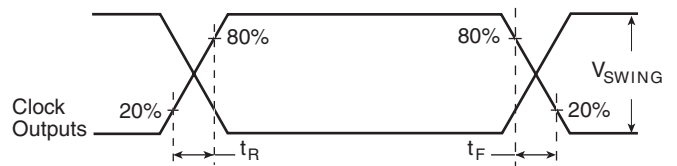
OUTPUT SKEW



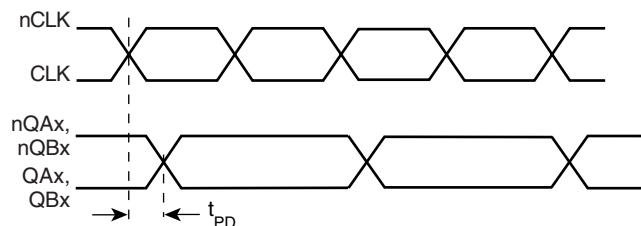
PART-TO-PART SKEW



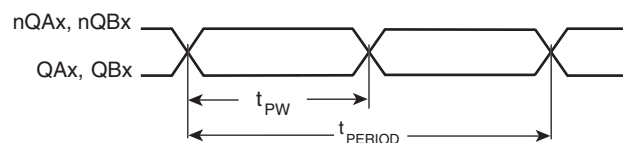
BANK SKEW



OUTPUT RISE/FALL TIME

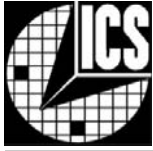


PROPAGATION DELAY



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

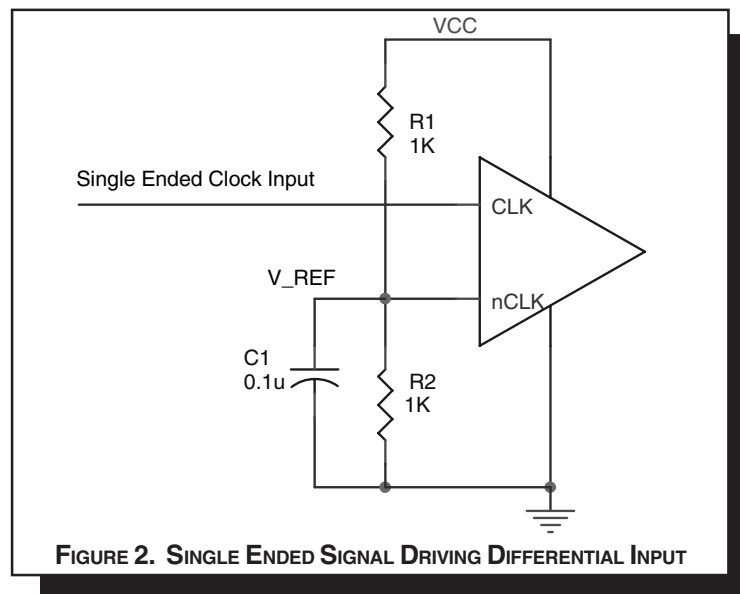
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3V$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.



RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.



DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please

consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

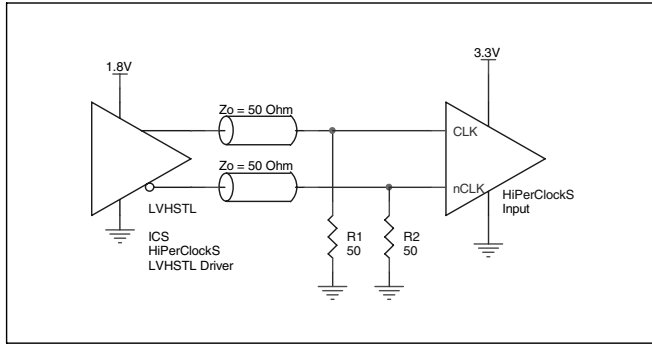


FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER

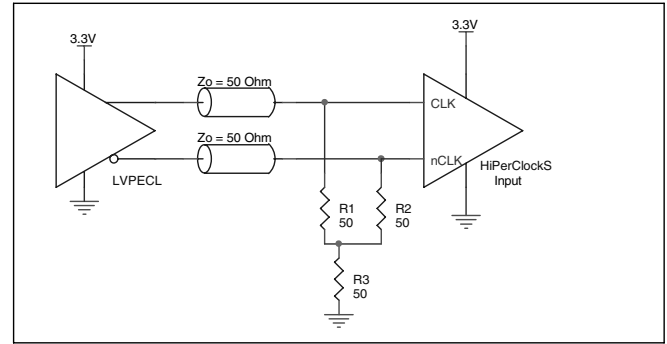


FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

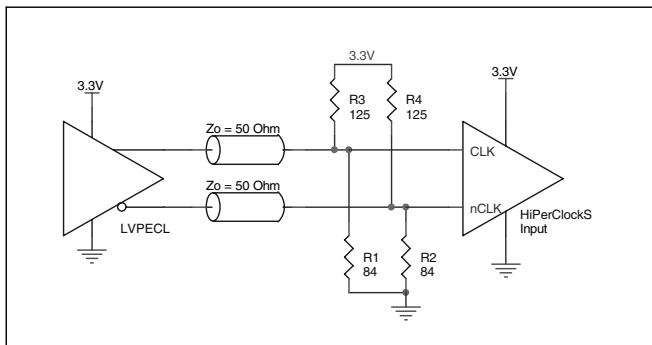


FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

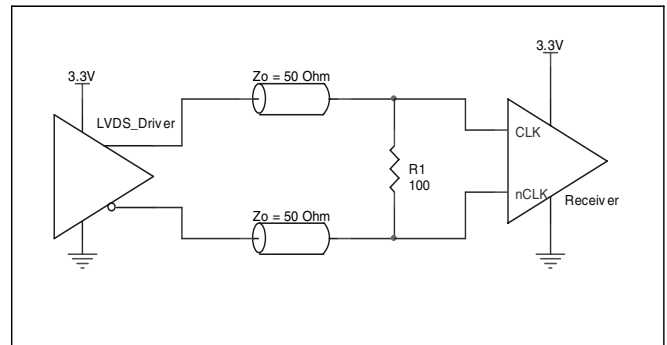


FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

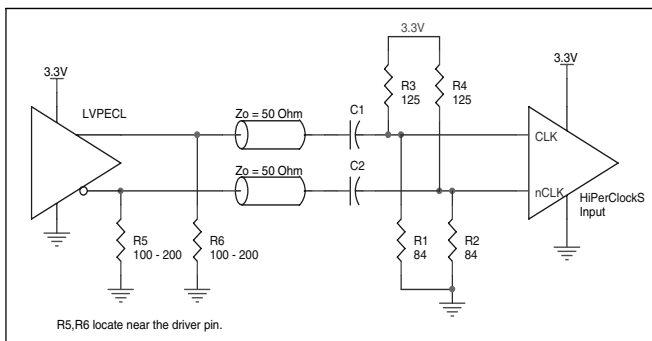


FIGURE 3E. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER WITH AC COUPLE



TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched imped-

ance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

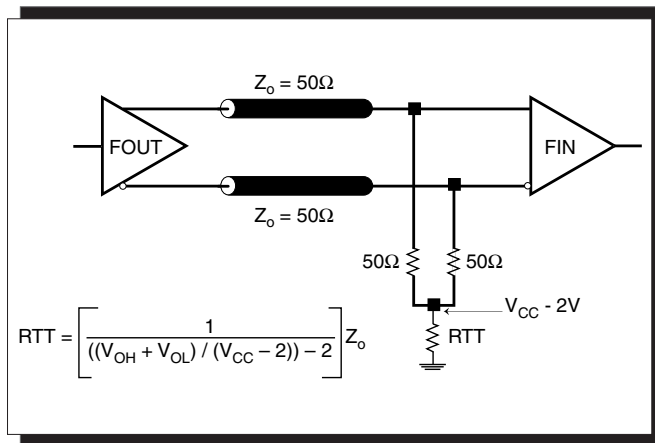


FIGURE 4A. LVPECL OUTPUT TERMINATION

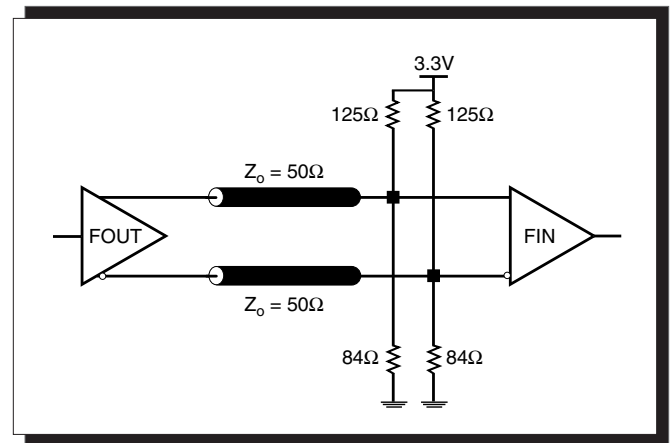


FIGURE 4B. LVPECL OUTPUT TERMINATION



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS87339-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS87339-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 0.3V = 3.6V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{CC_MAX} = 3.6V * 105mA = 378$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $4 * 30mW = 120mW$

Total Power_{MAX} (3.6V, with all outputs switching) = $378mW + 120mW = 498mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 6 below. Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$70^\circ C + 0.498W * 39.7^\circ C/W = 89.8^\circ C$. This is well below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN SOIC, FORCED CONVECTION

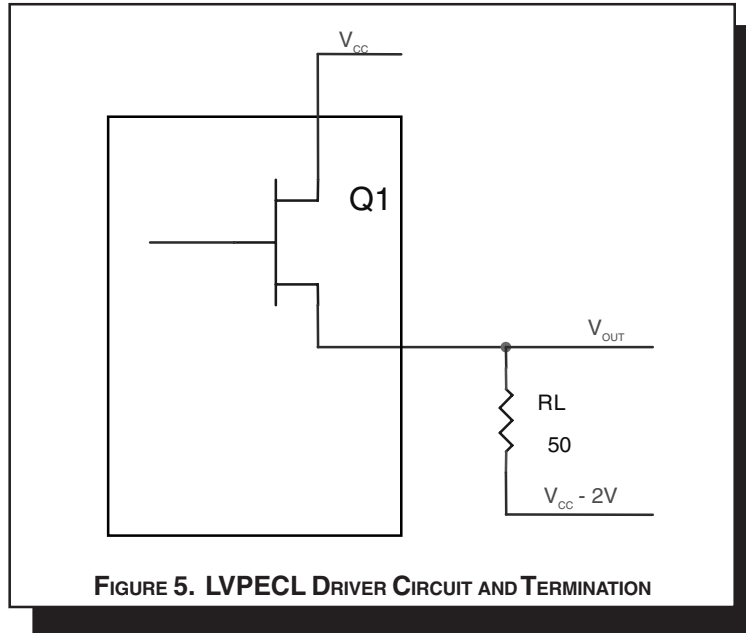
	θ_{JA} by Velocity (Linear Feet per Minute)		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 5*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$

$$(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$

$$(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = 30mW$



RELIABILITY INFORMATION

TABLE 7. θ_{JA} vs. AIR FLOW TABLE FOR 20 LEAD SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS87339-01 is: 1745

Compatible with MC100LVEL39



PACKAGE OUTLINE - M SUFFIX FOR 20 LEAD SOIC

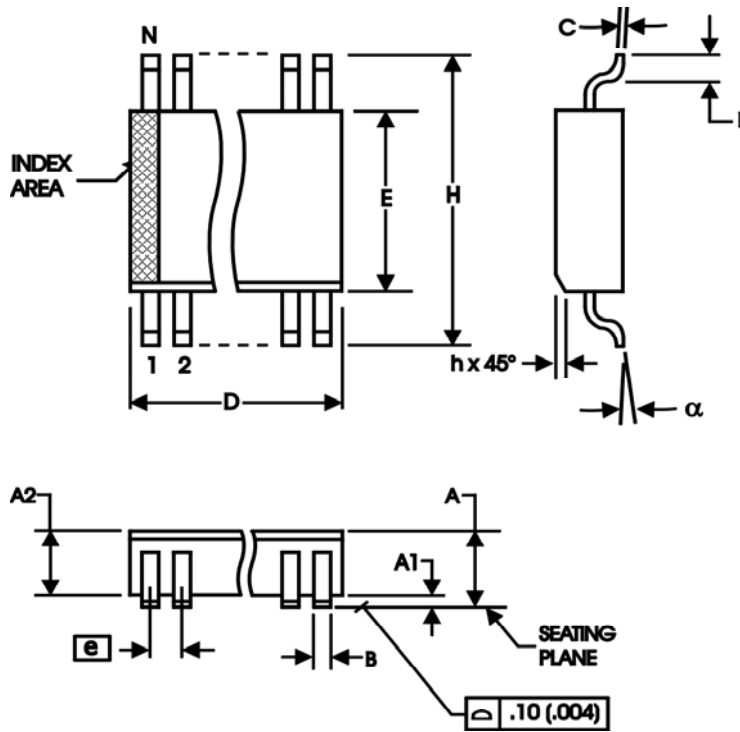


TABLE 8 PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119



Integrated
Circuit
Systems, Inc.

ICS87339-01

LOW SKEW, $\div 2/4, \div 4/6$,
DIFFERENTIAL-TO-3.3V LVPECL / ECL CLOCK GENERATOR

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS87339AM-01	ICS87339AM01	20 lead SOIC	Tube	0°C to 70°C
ICS87339AM-01T	ICS87339AM01	20 lead SOIC	1000 Tape & Reel	0°C to 70°C
ICS87339AM-01LF	ICS87339A01L	20 lead "Lead-Free" SOIC	Tube	0°C to 70°C
ICS87339AM-01LFT	ICS87339A01L	20 lead "Lead-Free" SOIC	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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